WHAT IS CLAIMED IS:

1. A method of fabricating a transistor having a source, drain, and a gate on a substrate, the method comprising:

implanting, into a surface of the substrate, a first impurity region (1904) with a first volume and a first surface area, the first impurity region being of a first type;

implanting, into a drain region of the transistor, a second impurity region (1912) with a second volume and a second surface area in the first surface area of the first impurity region, the second impurity region being of an opposite second type relative to the first type;

forming a gate oxide (1920) between a source region and the drain region of the transistor, the gate oxide of the transistor being formed after implantation of the second impurity region;

covering the gate oxide with a conductive material (1922);

implanting, into the source region of the transistor, a third impurity region (1916) with a third volume and a third surface area and a fourth impurity region (1918) with a fourth volume and a fourth surface area in the first surface area of the first impurity region, the third impurity region being of the opposite second type, the fourth impurity region being of the first type; and

implanting, into the drain region of the transistor, a fifth impurity region (1910) with a fifth volume and a fifth surface area in the second surface area of the second impurity region, the fifth impurity region being of the opposite second type.

2. The method of claim 1, wherein the transistor is a p-type LDMOS transistor.

3. The method of claim 1, wherein the second impurity region is a p-type double doped drain.

4. The method of claim 1, wherein the first impurity region is a conventional CMOS n-well.

5. A method of fabricating an NMOS transistor with floating operation capability, the NMOS transistor having a source, drain, and a gate on a substrate, the method

comprising:

implanting, into a surface of the substrate, an HV n-well (500B) with a first volume and a first surface area;

implanting, into the first surface area of the HV n-well, a P-body implant (700) with a second volume and a second surface area in the first surface area of the HV n-well;

implanting, into a drain region of the NMOS transistor, an n+ region (710) with a third volume and a third surface area in the P-body implant; and

implanting, into a source region of the NMOS transistor, an n+ region (712) with a third volume and a third surface area in the P-body implant.

6. A method of fabricating a PMOS transistor with floating operation capability, the PMOS transistor having a source, drain, and a gate on a substrate, the method comprising:

implanting, into a surface of the substrate, an HV n-well (500B) with a first volume and a first surface area;

implanting, into a source region of the PMOS transistor, a p+ region (526) with a second volume and a second surface area in the HV n-well; and

implanting, into a drain region of the PMOS transistor, a p+ region (528) with a third volume and a third surface area in the HV n-well.

7. A voltage regulator having an input terminal and an output terminal, the voltage regulator comprising:

a PMOS transistor connecting the input terminal to an intermediate terminal, the PMOS transistor including a first gate oxide layer;

an LDMOS transistor connecting the intermediate terminal to ground, the LDMOS transistor including a second gate oxide layer;

a controller that drives the PMOS transistor and the LDMOS transistor to alternately couple the intermediate terminal between the input terminal and ground to generate an intermediate voltage at the intermediate terminal having a rectangular waveform; and

a filter disposed between the intermediate terminal and the output terminal to convert

the rectangular waveform into a substantially DC voltage at the output terminal.

8. The voltage regulator of claim 1, wherein the controller drives the PMOS transistor with a first gate voltage and drives the LDMOS transistor with a second, different, gate voltage.

9. The voltage regulator of claim 8, wherein the second gate voltage is compatible with a CMOS logic circuit.

10. The voltage regulator of claim 1, wherein first gate voltage is larger than the second gate voltage.

11. The voltage regulator of claim 10, wherein the second gate oxide layer is thicker than the first gate oxide layer.

12. The voltage regulator of claim 1, wherein the PMOS transistor and the LDMOS transistor have a similar threshold voltage.

13. The voltage regulator of claim 1, wherein the PMOS transistor, the LDMOS transistor, and the controller are monolithically integrated onto a single chip.

14. The voltage regulator of claim 13, wherein the controller is fabricated using conventional CMOS transistor.

15. The voltage regulator of claim 1, wherein the PMOS transistor is a p-type LDMOS transistor.

16. The voltage regulator of claim 1, further comprising a PMOS driver to drive the PMOS transistor, and an LDMOS driver to drive the LDMOS transistor.

17. The voltage regulator of claim 16, wherein the PMOS driver is fabricated using conventional CMOS transistors.

18. The voltage regulator of claim 16, wherein the LDMOS driver is fabricated using conventional CMOS transistors.